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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

EJV

Office Action Summary	Application No.	Applicant(s)	
	10/814,866	DIORIO ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-72 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-72 is/are rejected.

7)☒ Claim(s) 12, and 66 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03/30/04 08/02/04 .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: See Continuation Sheet.

Continuation of Attachment(s) 6). Other: Information Disclosure Statements Mailing Dates: 02/10/05, 12/15/05, 1/23/06.

DETAILED ACTION

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Applicant is advised that should claims 12 and 66 be found allowable, claims 3 and 35 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-27, 29, 31-48, 54 and 56-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Goetteing et al. (USPN 6,529,407) (hereinafter Goetting)

With respect to claim 1, Goetting discloses in Fig. 2, "an electronic fuse (circuit of elements 207, 208, 209, 210, 100A and 100B in Fig. 2), comprising, a logic gate (either 205 or 206) and at least one nonvolatile memory element (either 100A or 100B), said at least one nonvolatile memory element configured to be programmed to a memory value capable of causing an input to said logic gate to settle to a predetermined state as a power-up or a reset signal is applied to the fuse (when the eq signal is pulsed either 100A or 100B is programmed to a value, which provide an input (based upon the difference of the thresholds of 100A and 100B) to 205 or 206 upon a recall procedure)."

With respect to claim 2, Goetting discloses, "the electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value (It can be seen in Fig. 1 that both 100A and 100B are composed of floating gate transistors, in which 205 and 206 are programmed based upon the threshold voltage of 100 A or 100B, which is controlled by their respective floating gates (FG))."

With respect to claim 3, Goetting discloses in Fig. 1, "the electronic fuse of Claim 2, wherein said nonvolatile memory element (100, which corresponds to 100A and 100B of Fig. 2) further comprises a first capacitor (101, is a PMOS transistor connected to function as a capacitor) having a first plate (gate of 101) in common with the floating gate (FG) of said floating-gate transistor (102)."

With respect to claim 4, Goetting discloses in Fig. 2, the electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process (it can be seen in both Fig. 1 and Fig. 2 that 100A and 100B are composed of MOSFET transistors, thus they are manufactured in a "MOS fabrication process")."

With respect to claim 5, Goetting discloses in Fig. 1, "the electronic fuse of Claim 2, wherein said floating-gate transistor is a MOS device (it can be seen that 102 of 100 is a NMOS transistor)."

With respect to claim 6, Goetting discloses in Fig. 1, the electronic fuse of Claim 1, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage (It is clear that 100A and 100B are composed of a capacitor connected PMOS transistor 101, which has an insulated gate, and thus the capacitor 100 has a dielectric property (a dielectric is an insulation between two electric poles, and 100 has insulting oxide (the dielectric) between p and n doped regions)."

With respect to claim 7, Goetting's floating gate transistor is capable of having its charge changed using Fowler-Nordheim tunneling.

With respect to claim 8, Goetting's floating gate transistor is capable of having its charge changed using hot-electron injection.

With respect to claim 9, Goetting's floating gate transistor is capable of having its charge changed using direct tunneling.

With respect to claim 10, Goetting's floating gate transistor is capable of having its charge changed using hot-hole injection.

With respect to claim 11, Goetting's floating gate transistor is capable of having its charge changed using ultraviolet radiation exposure.

With respect to claim 12, Goetting discloses in Fig. 1,"the electronic fuse of Claim 2, wherein said nonvolatile memory element (100, which corresponds to 100A and 100B of Fig. 2) further comprises a first capacitor (101, is a PMOS transistor connected to function as a capacitor) having a first plate (gate of 101) in common with the floating gate (FG) of said floating-gate transistor (102, of 100A and 100B)."

With respect to claim 13, Goetting discloses in Fig. 2, "the electronic fuse of Claim 12, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor (it can be seen in Fig. 2 that the fuse circuit comprises two floating gate transistors that are non-volatile memory elements 100A and 100B, which both have the capacitor connection. See rejection for claim 3)."

With respect to clam 14 Goetting discloses in Fig. 4A, a circuit comprising:

"a master fuse (circuit of elements 207, 208, 209, 210, 100A and 100B in Fig. 2, are present in the first latch, which receives the din of Fig. 4A) having a master latch (207 of Fig. 2, which again is present in the above latch device of Fig. 4A) and a nonvolatile memory element coupled between (100 A and 100B) a reset node (either node at drain or source of 208) of the master-slave electronic fuse and the master latch; and

a slave latch (200, latch that receives the output q of the above latch of Fig. 4A) having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal (q is output from the first latch, which input to d of 200 (the second latch)),

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node (when the eq signal is pulsed 207 latches to a state programmed to 100A and 100B, which is then output as q and then input to the d terminal of the second latch 200)."

With respect to claim 15, Goetting discloses, "the master-slave electronic fuse of Claim 14, wherein the predetermined state of said master latch is affected by a memory value to which the nonvolatile memory element is programmed (the state of the master latch is affected by the programmed difference in the threshold of 100A and 100B)."

With respect to claim 16, Goetting discloses, "the master-slave electronic fuse of Claim 15, wherein said master latch comprises cross-coupled inverters (207, is composed of cross-coupled inverters 205 and 06)."

With respect to claim 17, Goetting discloses, "the master-slave electronic fuse of Claim 15, wherein said nonvolatile memory element comprises a floating gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value (100A and 100B are both composed of the circuit of Fig. 1, which has a

floating gate transistor, and its programmed value is determined by the amount of charge present at its floating gate (FG of fig. 1))."

With respect to claim 18, Goetting discloses, "the master-slave electronic fuse of Claim 17, wherein said nonvolatile memory element (100, which corresponds to 100A and 100B of Fig. 2) further comprises a first capacitor (101, is a PMOS transistor connected to function as a capacitor) having a first plate (gate of 101) in common with the floating gate (FG) of said floating-gate transistor (102 of 100A or 100B)."

With respect to claim 19, Goetting discloses "the electronic fuse of Claim 14, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process (it can be seen in both Fig. 1 and Fig. 2 that 100A and 100B are composed of MOSFET transistors, thus they are manufactured in a "MOS fabrication process")."

With respect to claim 20, Goetting discloses, "the master-slave electronic fuse of Claim 17, wherein said floating-gate is a MOS device (Fig. 1 clearly shows that 100 is a MOS device)."

With respect to claim 21, Goetting discloses, the electronic fuse of Claim 14, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage (It is clear that 100A and 100B are composed of a capacitor connected PMOS transistor 101, which has an insulated gate, and thus the capacitor 100 has a dielectric property (a dielectric is an insulation between two electric poles, and 100 has insulting oxide (the dielectric) between p and n doped regions)."

With respect to claim 22, Goetting's floating gate transistor is capable of having its charge changed using Fowler-Nordheim tunneling.

With respect to claim 23, Goetting's floating gate transistor is capable of having its charge changed using hot-electron injection.

With respect to claim 24, Goetting's floating gate transistor is capable of having its charge changed using direct tunneling.

With respect to claim 25, Goetting's floating gate transistor is capable of having its charge changed using hot-hole injection.

With respect to claim 26, Goetting's floating gate transistor is capable of having its charge changed using ultraviolet radiation exposure.

With respect to claim 27, Goetting discloses, "the electronic fuse of Claim 17, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor (it can be seen in Fig. 2 that the fuse circuit comprises two floating gate transistors that are non-volatile memory elements 100A and 100B, which both have the capacitor connection. See rejection for claim 3)."

With respect to claim 29, Goetting discloses, "the master slave electronic fuse of claim 17, wherein the master latch is predisposed to settle into said first sate when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low (The charge on the floating gate of 100A and 100B dictates the programmed state of the nonvolatile memory, which in turn will be used to program master latch 207. See Col. 3 lines 16-27)."

With respect to claim 31, Goetting discloses, "the master-slave electronic fuse of claim 29, wherein said master latch comprises cross-coupled inverters (205 and 206 of latch 207) and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to- length ratio of at least one of the transistors of a second one of said cross-coupled inverters (it can be seen that the gate-width-to-length ratio of the PMOS transistor of 205 is 10/1.1, which is larger than the gate-width-to-length ratio of 3/1.1 of the NMOS transistor of inverter 206)."

With respect to claim 32, Goetting discloses, "the master-slave electronic fuse of claim 29, wherein said master latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters (it can be seen in Fig. 2, that inverters 205 and 206 of latch 207 have different transistor sizes. Thus, the larger gate width PMOS transistors would require more doping than smaller gate width NMOS transistors. Therefore, The PMOS transistor of 205 would require a larger doping level than the NMOS transistor of 206.)."

With respect to claim 33, Goetting discloses, in Fig. 2, "a master-slave electronic fuse, comprising:

(circuit of elements 207, 208, 209, 210, 100A and 100B in Fig. 2, are present in the first latch, which receives the din of Fig. 4A) having a master latch (207 of Fig. 2, which again is present in the above latch device of Fig. 4A) and a nonvolatile memory

element (100 A) coupled between a reset node (gate of 208) of the master-slave electronic fuse and a first node of a master latch (node at connected to 208 and 209), and a second nonvolatile memory element coupled between the reset node (gate of 208) and a second node (node that connects 208 and 210) of the master latch (207).

a slave latch (200, latch that receives the output q of the above latch of Fig. 4A) having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal (q is output from the first latch, which input to d of 200 (the second latch)),

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node (when the eq signal is pulsed 207 latches to a state programmed to 100A and 100B, which is then output as q and then input to the d terminal of the second latch 200)."

With respect to claim 34, Goetting discloses, "the master-slave electronic fuse of Claim 33, wherein the predetermined state of said master latch is affected by a reset memory value associated with the first nonvolatile memory element (When eq signal is pulsed the value programmed into 100A is used to set the latch value to the value programmed into 100A)."

With respect to claim 35, Goetting discloses, "the master-slave electronic fuse of Claim 33, wherein the predetermined state of said master latch is affected by a reset memory value associated with the second nonvolatile memory element (When eq signal

is pulsed the value programmed into 100B is used to set the latch value to the value programmed into 100B)."

With respect to claim 36, Goetting discloses, "the master-slave electronic fuse of Claim 34, wherein said nonvolatile memory element comprises a first floating gate transistor having a first floating gate, an amount of charge on the first floating gate determining said memory value (100A and 100B are both composed of the circuit of Fig. 1, which has a floating gate transistor, and its programmed value is determined by the amount of charge present at its floating gate (FG of fig. 1))."

With respect to claim 37, Goetting discloses, "the master-slave electronic fuse of Claim 35, wherein said nonvolatile memory element comprises a second floating gate transistor having a second floating gate, an amount of charge on the second floating gate determining said memory value (100A and 100B are both composed of the circuit of Fig. 1, which has a floating gate transistor, and its programmed value is determined by the amount of charge present at its floating gate (FG of fig. 1))."

With respect to claim 38, Goetting discloses, "the master-slave electronic fuse of claim 35, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value and wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, and amount of charge on the second floating gate determining said second memory value (100A and 100B are both composed of the circuit of Fig. 1, which has a floating gate transistor, and its programmed value is determined by the amount of charge present at

its floating gate (FG of fig. 1). Further 100A and 100B are programmed to different values that will be used to control the latch circuit. See Col. 3 lines 35-52)."

With respect to claim 39, Goetting discloses, "the master-slave electronic fuse of Claim 38, wherein said first nonvolatile memory element (100, which corresponds to 100A and 100B of Fig. 2) further comprises a first capacitor (101, is a PMOS transistor connected to function as a capacitor) having a first plate (gate of 101) in common with the floating gate (FG) of said floating-gate transistor (102 of 100A or 100B)."

With respect to claim 40, Goetting discloses, "the master-slave electronic fuse of Claim 39, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor (it can be seen in Fig. 2 that the fuse circuit comprises two floating gate transistors that are non-volatile memory elements 100A and 100B, which both have the capacitor connection. See rejection for claim 39)."

With respect to claim 41, clearly the all of the transistors in Goetting are MOS transistors, thus they are manufactured in a MOS fabrication process.

With respect to claim 42, it can be seen in Fig. 1 that the floating gate transistors are MOS transistors.

With respect to 43, Goetting discloses, "the electronic fuse of Claim 33, wherein at least one of said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage (It is clear that 100A and 100B are composed of a capacitor connected PMOS transistor 101, which has an insulated gate, and thus the

capacitor 100 has a dielectric property (a dielectric is an insulation between two electric poles, and 100 has insulting oxide (the dielectric) between p and n doped regions)."

With respect to claim 44, Goetting's floating gate transistor is capable of having its charge changed using Fowler-Nordheim tunneling.

With respect to claim 45, Goetting's floating gate transistor is capable of having its charge changed using hot-electron injection.

With respect to claim 46, Goetting's floating gate transistor is capable of having its charge changed using direct tunneling.

With respect to claim 47, Goetting's floating gate transistor is capable of having its charge changed using hot-hole injection.

With respect to claim 48, Goetting's floating gate transistor is capable of having its charge changed using ultraviolet radiation exposure.

With respect to claim 54, "the master slave electronic fuse of claim 38, wherein the master latch is predisposed to settle into one of said first and second sates in response to said first and second memory values. (The charge on the floating gate of 100A and 100B dictates the programmed state of the nonvolatile memory, which in turn will be used to program master latch 207. See Col. 3 lines 16-27)."

With respect to claim 56, Goetting discloses, "the master-slave electronic fuse of claim 54, wherein said master latch comprises cross-coupled inverters (205 and 206 of latch 207) and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to- length ratio of at least one of the transistors of a second one of said cross-coupled inverters (it can

be seen that the gate-width-to-length ratio of the PMOS transistor of 205 is 10/1.1, which is larger than the gate-width-to-length ratio of 3/1.1 of the NMOS transistor of inverter 206)."

With respect to claim 57, Goetting discloses, "the master-slave electronic fuse of claim 54, wherein said master latch comprises cross-coupled inverters and wherein a first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters (it can be seen in Fig. 2, that inverters 205 and 206 of latch 207 have different transistor sizes. Thus, the larger gate width PMOS transistors would require more doping than smaller gate width NMOS transistors. Therefore, The PMOS transistor of 205 would require a larger doping level than the NMOS transistor of 206.)."

With respect to clam 58 Goetting discloses in Fig. 4A, a circuit comprising:

"a master fuse (circuit of elements 205, 206, 208, 209, 210, 100A and 100B in Fig. 2, are present in the first latch, which receives the din of Fig. 4A) having a logic gate (205 or 206 of Fig. 2, which again is present in the above latch device of Fig. 4A) and a nonvolatile memory element coupled between (100 A and 100B) a reset node (either node at drain or source of 208); and

a slave latch (200, latch that receives the output q of the above latch of Fig. 4A) having a slave-latch input coupled to an output of the master fuse (q) and a slave-latch node configured to receive a slave-latch signal (q is output from the first fuse, which input to d of 200 (the second latch)),

wherein said logic-gate element is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the logic-gate element upon application of a slave-latch signal to the slave-latch node (when the eq signal is pulsed 207 latches to a state programmed to 100A and 100B, which is then output as q and then input to the d terminal of the second latch 200)."

With respect to claim 59, Goetting discloses, "the master-slave electronic fuse of Claim 58, wherein the predetermined state of said logic-gate element is affected by a memory value to which the nonvolatile memory element is programmed (the state of the logic-gate element is affected by the programmed difference in the threshold of 100A and 100B)."

With respect to claim 60, Goetting discloses, "the master-slave electronic fuse of Claim 59, wherein said nonvolatile memory element comprises a floating gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value (100A and 100B are both composed of the circuit of Fig. 1, which has a floating gate transistor, and its programmed value is determined by the amount of charge present at its floating gate (FG of fig. 1))."

With respect to claim 61, Goetting discloses, "the master-slave electronic fuse of Claim 60, wherein said nonvolatile memory element (100, which corresponds to 100A and 100B of Fig. 2) further comprises a first capacitor (101, is a PMOS transistor connected to function as a capacitor) having a first plate (gate of 101) in common with the floating gate (FG) of said floating-gate transistor (102 of 100A or 100B)."

With respect to claim 62, Goetting discloses "the electronic fuse of Claim 58, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process (it can be seen in both Fig. 1 and Fig. 2 that 100A and 100B are composed of MOSFET transistors, thus they are manufactured in a "MOS fabrication process")."

With respect to claim 63, Goetting discloses, "the master-slave electronic fuse of Claim 60, wherein said floating-gate is a MOS device (Fig. 1 clearly shows that 100 is a MOS device)."

With respect to claim 64, Goetting discloses, the electronic fuse of Claim 58, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage (It is clear that 100A and 100B are composed of a capacitor connected PMOS transistor 101, which has an insulated gate, and thus the capacitor 100 has a dielectric property (a dielectric is an insulation between two electric poles, and 100 has insulting oxide (the dielectric) between p and n doped regions)."

With respect to claim 65, Goetting's floating gate transistor is capable of having its charge changed using Fowler-Nordheim tunneling.

With respect to claim 66, Goetting's floating gate transistor is capable of having its charge changed using Fowler-Nordheim tunneling.

With respect to claim 67, Goetting's floating gate transistor is capable of having its charge changed using hot-electron injection.

With respect to claim 68, Goetting's floating gate transistor is capable of having its charge changed using direct tunneling.

With respect to claim 69, Goetting's floating gate transistor is capable of having its charge changed using hot-hole injection.

With respect to claim 70, Goetting's floating gate transistor is capable of having its charge changed using ultraviolet radiation exposure.

With respect to claim 71, Goetting discloses, "the electronic fuse of Claim 61, wherein the nonvolatile memory element further comprises a second capacitor having a first plate in common with the floating gate of said floating-gate transistor (it can be seen in Fig. 2 that the fuse circuit comprises two floating gate transistors that are non-volatile memory elements 100A and 100B, which both have the capacitor connection. See rejection for claim 3)."

With respect to claim 72, Goetting discloses, "the master slave electronic fuse of claim 60, wherein the logic-gate element is predisposed to settle into said first sate when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low (The charge on the floating gate of 100A and 100B dictates the programmed state of the nonvolatile memory, which in turn will be used to program logic-gate element 207. See Col. 3 lines 16-27)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28, 30, 51-52, and 55 rejected under 35 U.S.C. 103(a) as being unpatentable over Goetting et al. (USPN 5,912,937) in view of Pascucci et al (5,659,498). Goetting et al. teaches the circuits of claims 14, 29, 41, 38, and 54 (see above rejections under 35 USC § 102 (b)). Goetting et al. does not teach the required capacitor and latch output connections. However, Pascucci et al. teaches, in Fig. 1, a latch circuit with capacitors (13, 12) attached to the outputs of a cross-coupled inverter latch and fixed voltages. Pascucci et al.'s is a latch used in a fused circuit to further reduce the possibility of accidental programming and has reduced power consumption when the fuse has not yet been programmed.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the un balanced cross-coupled inverter latch of Pascucci et al., in place of the cross coupled inverter latch 207 of Goetting et al. for the purpose of having a latch capable of preventing a false program, and has reduced power consumption. One skilled in the art would have been motivated to use Pascucci et al.'s latch of Fig. 1 in place of Goetting et al.'s latch 207 to lessen power consumption, and the chance of a false programming occurrence in Goetting et al.'s circuit of Fig. 2.

With respect to claim 28, the above combination discloses, "the master-slave electronic fuse of claim 14, further comprising a capacitive element coupled to an output

of the master latch (207 as modified above has a capacitor 12, or 13 coupled to an output node 6 or 7.)."

With respect to claim 30, the above combination discloses, "the master-slave electronic fuse of claim 29, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source. (in modified latch 207 element 13 is a capacitor coupled to output 7 and voltage source Vdd. Additionally, 12 is also a capacitor coupled to output 6 and voltage source ground.)"

With respect to claim 51, the above combination discloses, "the master-slave latch of claim 38, wherein a first output of said master latch is capacitively coupled to a first source of a fixed voltage (in modified latch 207 element 13 is a capacitor coupled to output 7 and voltage source Vdd)."

With respect to claim 52, the above combination discloses, "the master-slave latch of claim 51, wherein a second output of said master latch is capacitively coupled to a second source of a fixed voltage (in modified latch 207 element 12 is a capacitor coupled to output 6 and voltage source ground)."

Claims 51-53, are rejected under 35 U.S.C. 103(a) as being unpatentable over Goetting et al. (USPN 5,912,937) in view of Hartgring et al. (5,086,331). Goetting et al. teaches the circuit of claim 38 (see above rejections under 35 USC § 102 (b)). Goetting et al. does not teach the required capacitor and latch output connections. However, Hartgring et al. teaches, in Fig. 3, a latch circuit with capacitors (Cp, Cout) attached to the outputs of a cross-coupled inverter latch and fixed voltages. Hartgring et al.'s is a latch allows for the use of smaller transistors.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the latch of Hartgring et al., in place of the latch 207 of Goetting et al. to reduce the size of the transistors used in Goetting et al.'s circuit. One skilled in the art would have been motivated to use Hartgring et al.'s latch of Fig. 1 in place of Goetting et al.'s latch 207 to obtain an efficient packaging of the transistors, and thus an efficient chip deign of Goetting et al's circuit.

With respect to claim 51, the above combination discloses, "the master-slave latch of claim 38, wherein a first output of said master latch is capacitively coupled to a first source of a fixed voltage (in modified latch 207 element Cp is a capacitor coupled to output 5 and voltage source ground)."

With respect to claim 52, the above combination discloses, "the master-slave latch of claim 51, wherein a second output of said master latch is capacitively coupled to a second source of a fixed voltage (in modified latch 207 element Cout is a capacitor coupled to output 7 and voltage source ground)."

With respect to claim 53 it cab be seen that both Cp and Cout are coupled to ground.

Claims 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goetting et al. (USPN 5,912,937) in view of Caywood (6,384,451). Goetting et al. teaches the circuits of claims 41 (see above rejections under 35 USC § 102 (b)). Goetting et al. does not teach the required third and fourth capacitor in the non-volatile memory circuit. However, Caywood teaches, in Fig. 5, a nonvolatile circuit with capacitive elements (50, and 30) attached to a floating gate transistor (150). Caywood's

the capacitive elements 50 and 30 of the non-volatile memory floating gate transistors allow for designing smaller and lower voltage floating gate transistors circuits.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use Caywood's smaller, lower voltage nonvolatile memory floating gate transistors 150 in place of the floating gate transistors 100A and 100B of Goetting et al. for the purpose having nonvolatile memory elements that are smaller and require less voltage. Thus, allowing for more space efficient circuit design, that uses less voltage and thus consumes less power. One skilled in the art would have been motivated to use Caywood's nonvolatile memory of Fig. 5 in place of Goetting et al.'s nonvolatile memory 100A and 100B to lessen power consumption, and required chip space in Goetting et al.'s fuse circuit.

With respect to claim 49, the above combination discloses, "the master-slave electronic fuse of Claim 41, wherein the first nonvolatile memory element further comprises a third capacitor having a first plate in common with the first floating gate of said first floating-gate transistor (150 in place of 100A would have a first capacitor 50 and a third capacitor 30 coupled to the gate of floating gate transistor of 150.)."

With respect to claim 50, the above combination discloses, "the master-slave electronic fuse of Claim 41, wherein the first nonvolatile memory element further comprises a fourth capacitor having a first plate in common with the second floating gate of said first floating-gate transistor (150 in place of 100B would have a second capacitor 50 and a fourth capacitor 30 coupled to the gate of floating gate transistor of 150.)."

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Cosetello et al. (USPN 6,822,864) discloses, in Fig. 2, capacitors coupled to the outputs of inverters in a cross-coupled inverter latch.

Shukuri (USPN 6,724,657) disclose in Fig. 4, a fuse circuit with a nonvolatile memory and latch circuit.

Yokozeki (USPGPN 2003/0123276) discloses, in Fig. 1, a cross-coupled inverter latch with capacitors coupled to the outputs of the inverters to ground.

Hirano (USPN 6,111,785) discloses, in Fig. 5, a fuse circuit with a nonvolatile memory cross-coupled inverter latch, and a reset signal.

Kim (USPN 5,912,841) discloses a fuse circuit with a nonvolatile latch.

Rao et al. (USPN 5,835,402) disclose in Fig. 1 a single floating gate memory device coupled to a latch, and in Fig. 5, discloses two floating gate memory devices programming an output latch.

Wheelus et al. (5,677,917) discloses, in Fig. 1, a master fuse circuit controlling a slave latch.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am

to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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